What is claimed is:

1. A processor, having a plurality of instruction slots each of which stores an instruction to be executed in parallel, wherein one of the plurality of instruction slots is a first instruction slot and another one of the plurality of instruction slots is a second instruction slot, the processor being characterized by:

a special instruction stored in the first instruction slot being executed by a first functional unit that executes instructions stored in the first instruction slot and a second functional unit that executes instructions stored in the second instruction slot, while an instruction in the second instruction slot is executed by a third functional unit that executes instructions stored in the second instruction slot.

2. The processor of Claim 1, wherein:

the special instruction denotes addition and subtraction, and

one of the first and second functional units performs addition and the other subtraction, as denoted by the special instruction.

1   3. The processor of Claim 2, wherein the instruction is a

2   multiply instruction, and the third functional unit is a

3   multiplier.

1   4. A processor for executing a plurality of instructions

2   in parallel, comprising:

3   an instruction register having at least first and second

4   instruction slots, for storing the plurality of instructions;

5   first and second decoders, for respectively decoding the

6   instructions stored in the first and second instruction slots;

7   first and second functional units, which, if a special

8   instruction is decoded by the first decoder, together execute

9   the special instruction under the control of the first decoder;

10   and

11   a third functional unit, for executing an instruction in

12   parallel with the execution of the special instruction, under

13   the control of the second decoder.

1   5. The processor of Claim 4, wherein:

2   the special instruction denotes addition and subtraction,

3   and

4   one of the first and second functional units performs

5   addition and the other subtraction, as denoted by the special

6   instruction.

1   6.   The processor of Claim 5, wherein the instruction is a

2   multiply instruction, and the third functional unit is a

3   multiplier.

1   7.   A processor, for executing a plurality of instructions

2   in parallel, comprising:

3   a first and second decoding means, each of which decodes

4   instructions and generates decode results denoting the content

5   of the instructions, wherein, if the first decoding means

6   decodes a special instruction, the first decoding means

7   generates a first-part decode result denoting a first-type

8   calculation and a second-part decode result denoting a second-

9   type calculation;

10   a first and second executing means, corresponding to each

11 of the first and second decoding means, for executing

12 instructions in parallel according to a decode result from the

13 corresponding decoding means; and

14   a selecting means, for selecting the second-part decode

15 result if the first decoding means decodes the special

16   instruction, and selecting the decode result from the second

17   decoding means if the first decoding means decodes an

18   instruction other than the special instruction,

19   wherein the second executing means includes:

20   a first functional unit, which executes instructions

21   according to the decode result selected by the selecting means;

22   and

23   a second functional unit, which executes instructions

24   according to the decode result of the second decoding means,

25   and wherein, if the special instruction is decoded, the

26   first executing means performs a first-type calculation, and,

27   in the second executing means, the first functional unit

28   performs a second-type calculation and the second functional

29   unit executes an instruction other than a special instruction,

30   decoded by the second decoding means.

1   8.   The processor of Claim 7, wherein:

2   the special instruction includes an operation code denoting

3   the first-type calculation and the second-type calculation, and

4   first and second operands;

5   the first executing means performs the first-type

6   calculation on the first and second operands, and stores a

7   calculation result in the first operand;

8   the second executing means performs the second-type

9   calculation on the first and second operands, and stores a

10   calculation result in the second operand.

1   9.   The processor of Claim 8, wherein:

2   the first executing means includes an adder/subtracter;

3   the first functional unit is an adder/subtracter; and

4   the special instruction denotes addition as the first-type

5   calculation and subtraction as the second-type calculation.

1   10.   The processor of Claim 9, wherein the second

2   functional unit is a multiplier and the instruction is a

3   multiply instruction.

1   11.   The processor of Claim 9, wherein the second

2   functional unit is a data transfer unit and the instruction is

3   a transfer instruction.

1   12.   A processor that fetches long-word instructions, each

2   comprising at least two instructions, from a program, and

3   executes a plurality of instructions in parallel, wherein the

4   program includes special instructions for indicating a first-

5   type calculation and a second-type calculation, the processor

6   comprising:

7   an instruction register having first and second instruction

8   slots, for storing each of the instructions in a long-word

9   instruction;

10   a first decoding means, for decoding an instruction stored

11   in the first slot, and if the instruction is a special

12   instruction, generating a first decode result and a second

13   decode result;

14   a first executing means, for executing an instruction in

15   accordance with the first decode result;

16   a second decoding means, for decoding an instruction stored

17   in the second slot and generating a third decode result in

18   parallel with the decoding and generating performed by the

19   first decoding means;

20   a selecting means, for selecting the second decode result

21   if the special instruction is decoded by the first decoding

22   means, and selecting the third decode result if an instruction

23   other than a special instruction is decoded by the first

24   decoding means; and

25   a second executing means, for executing an instruction

26   according to the decode result selected by the selecting means,

27   wherein the first executing means performs the first-type

28   calculation if the special instruction is decoded by the first

29   decoding means; and

30   the second executing means performs the second-type

31   calculation if the second decode result is selected by the

32   selecting means.

1   13.   The processor of Claim 12, wherein:

2   the special instruction includes an operation code denoting

3   the first-type calculation and the second-type calculation, and

4   first and second operands;

5   the first executing means performs the first-type

6   calculation on the first and second operands, and stores a

7   calculation result in the destination indicated by the first

8   operand;

9   the second executing means performs the second-type

10   calculation on the first and second operands, and stores a

11   calculation result in the destination indicated by the second

12   operand.

1   14.   The processor of Claim 13, wherein the second

2   executing means includes:

3   a first functional unit, which executes an instruction

4   according to a decode result selected by the selecting means;

5   and

6   a second functional unit, which executes an instruction

7   according to the third decode result of the second decoding

8   means,

9   wherein the first functional unit performs the second-type

10   calculation according to the special instruction, and the

11   second functional unit executes an instruction other than a

12   special instruction in parallel with the special instruction

13   according to the third decode result.

1   15.   The processor of Claim 14, wherein:

2   the first executing means includes an adder/subtracter;

3   the first functional unit is an adder/subtracter; and

4   the special instruction denotes addition as the first-type

5   calculation and subtraction as the second-type calculation.

1   16.   The processor of Claim 15, wherein the second

2   functional unit is a multiplier and the instruction is a

3   multiply instruction.

17. The processor of Claim 15, wherein the second functional unit is a data transfer unit and the instruction is a transfer instruction.

18. A program conversion apparatus that changes a source program to an object program for a target processor executing long-word instructions, comprising:

a retrieving means, for retrieving a pair of instructions from the source program, the pair of instructions comprising a first instruction denoting a first-type calculation of two variables and a second instruction indicating a second-type calculation of the same two variables;

a generating means, for generating a special instruction corresponding to the retrieved pair, the special instruction comprising an operation code denoting the first-type calculation and the second-type calculation, and two operands representing the two variables,

an arranging means, for arranging the generated special instruction into a long-word instruction.

19. The program conversion apparatus of Claim 18, wherein

2   the first instruction denotes addition, and the second

3   instruction denotes subtraction.

1   20. The program conversion apparatus of Claim 19, wherein:

2   the target processor includes a first instruction execution

3 unit having a first calculation unit, and a second instruction

4 execution unit having a second calculation unit and a

5 multiplication unit, and

6   the arranging means retrieves a multiply instruction that

7 does not share dependency with the special instruction

8 generated by the generating means, and arranges the special

9 instruction and the multiply instruction into one long-word

10 instruction.